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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TARO FUJII, KOICHIRO FURUTA, MASATO MOTOMURA, KENICHIRO ANJO, YOSHIKAZU YABE, TORU AWASHIMA, TAKAO TOI, and NORITSUGU NAKAMURA

Appeal 2009-011862
Application 10/694,822
Technology Center 2100

Before JOSEPH L. DIXON, HOWARD B. BLANKENSHIP, and THU A. DANG, *Administrative Patent Judges*.

BLANKENSHIP, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 9, 15, and 21-35. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm-in-part.

Invention

Appellants' invention relates to an array-type processor in which the operations of a multiplicity of processor elements are controlled by a state control unit. Spec. 1: 4-9.

Representative Claims

9. An array-type processor, comprising:

a multiplicity of processor elements which individually execute data processing and supply event data as output in accordance with instruction codes for which data are individually set, said multiplicity of processor elements being arranged in rows and columns;

a plurality of state control units that intercommunicate to realize linked operation as necessary;

an event distributing means for distributing said event data to said plurality of state control units; and

a central control unit for distributing said event data to said plurality of state control units, said central control unit is surrounded by said plurality of state control units and is connected by said event distributing means to all of said plurality of state control units,

wherein said instruction codes of said multiplicity of processor elements are successively switched by said plurality of state control units in accordance with a computer program that has been installed in advance and in accordance with said event data,

wherein said event data are data for causing a transition of a current state that is controlled by the plural state control units and is composed of data for reporting to other state control units the current state that is being controlled by a particular state control unit.

15. An array-type processor, comprising:

a multiplicity of processor elements which individually execute data processing and supply event data as output in accordance with instruction codes for which data are individually set, said multiplicity of processor elements being arranged in rows and columns;

a plurality of state control units that intercommunicate to realize linked operation as necessary; and

an event distributing means for distributing said event data to said plurality of state control units,

wherein said instruction codes of said multiplicity of processor elements are successively switched by said plurality of state control units in accordance with a computer program that has been installed in advance and in accordance with said event data,

wherein said multiplicity of processor elements is divided into element areas so that there is a state control unit for each element area and there is one state control unit for a plurality of processor elements,

wherein each of said plurality of state control units is connected to said processor elements of a respective element area of said plurality of element areas, and

wherein said event distributing means transmits said event data that are supplied as output by said processor elements of each element area to a respective state control unit of said state control units, said event data are data for causing a transition of a current state that is controlled by the plural sate control units and is composed of data for reporting to other state control units the current state that is being controlled by a particular state control unit.

Examiner's Rejections/Claim Status

Claim 9 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Katsuki (US 5,581,767) "in view of common art" (Ans. 11).

Claims 15, 21, 23-25, 30, 32, 33, and 35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Katsuki and Stokes (US 3,537,074).

Claims 22, 26-29, 31, and 34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Katsuki, Stokes, and May (US 6,414,368 B1).

Claim 1 stands allowed. Claims 2-8, 10-14, and 16-20 have been canceled.

ANALYSIS

Claim 9

Instant claim 9 recites "a central control unit for distributing said event data to said plurality of state control units, said central control unit is surrounded by said plurality of state control units and is connected by said event distributing means to all of said plurality of state control units." According to Appellants, this "configuration" recited in claim 9 centralizes the data for uniform distribution, citing Specification page 21, line 22 to page 22, line 9. Appellants in the Reply Brief place emphasis on page 22, lines 3 through 5 of the Specification, which recites: "Distributing event data from central control unit 155 to all state control units 101 facilitates the realization of uniform linked operation in all state control units 101. . . ." According to Appellants, the two bus structures taught by Katsuki "teaches away" from a configuration in which there is a "uniform distribution."

Appellants also argue that modifying Katsuki to have a central control unit surrounded by a plurality of processors would require all the bus structures to be the same, which would change the basic principle under which Katsuki was designed to operate.

The *claims* measure the invention. *See SRI Int'l v. Matsushita Elec. Corp.*, 775 F.2d 1107, 1121 (Fed. Cir. 1985) (en banc). During prosecution before the USPTO, claims are to be given their broadest reasonable interpretation, and the scope of a claim cannot be narrowed by reading disclosed limitations into the claim. *See In re Morris*, 127 F.3d 1048, 1054 (Fed. Cir. 1997); *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989); *In re Prater*, 415 F.2d 1393, 1404-05 (CCPA 1969). Our reviewing court has repeatedly warned against confining the claims to specific embodiments described in the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005) (en banc).

"Giving claims their broadest reasonable construction 'serves the public interest by reducing the possibility that claims, finally allowed, will be given broader scope than is justified.'" *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004) (quoting *In re Yamamoto*, 740 F.2d 1569, 1571 (Fed. Cir. 1984)). "An essential purpose of patent examination is to fashion claims that are precise, clear, correct, and unambiguous. Only in this way can uncertainties of claim scope be removed, as much as possible, during the administrative process." *Zletz*, 893 F.2d at 322. "Construing claims broadly during prosecution is not unfair to the applicant . . . because the applicant has the opportunity to amend the claims to obtain more precise claim coverage." *American Academy,* 367 F.3d at 1364.

We agree with the Examiner that Appellants have failed to show that claim 9 requires the "uniform distribution" alleged to be missing from Katsuki. Appellants have not explained how the language of the claim might require a "uniform distribution," but merely point to written description in the Specification as support for Appellants' view.

In addition, Appellants have not offered sufficient evidence or reasoning in support of the allegation that modifying Katsuki to have a central control unit surrounded by a plurality of processors would require all the bus structures to be the same.

Accordingly, we are not persuaded that the Examiner erred in the rejection of claim 9. We sustain the Examiner's § 103(a) rejection of the claim.

Claims 15 and 21-35

Instant claim 15 recites "wherein said multiplicity of processor elements is divided into element areas so that there is a state control unit for each element area and there is one state control unit for a plurality of processor elements." Appellants argue that the § 103(a) rejection over Katsuki and Stokes errs because modifying Katsuki such that there is not a one-to-one correspondence between processors and control units would change the basic principle under which Katsuki was designed to operate.

Katsuki teaches a control/memory section that comprises arrays of control/memory units corresponding one-to-one to the processor units. Katsuki Abstract. As depicted in Figure 1 and described principally at column 7, line 23 through column 8, line 4, the reference teaches the use of two different buses. Transfer of information between adjacent processors is

via one bus. Transfer of information to a processor not adjacent is via a second bus and further transferred to the destination processor by an array of control/memory units 22 which are in a one-to-one correspondence with the processor units 12.

The Examiner does not respond to the argument that the proposed modification of Katsuki would change the basic principle of operation of the reference.[1] The rejection of claim 15 could be reversed on the basis of the lack of response to Appellants' argument alone.

The Examiner appears to respond to a "teaching away" argument not made in the Appeal Brief. The Examiner cites *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994), for the supposed proposition that a reference "teaches away" when it states that something cannot be done. The Examiner submits that Appellants have not satisfied "this burden" by showing "explicit language" in Katsuki that a many-to-one processor/control correspondence cannot be done. Ans. 16-17.

We agree with Appellants, as noted in the Reply Brief, that a reference does not "teach away" from the invention only when it states that something cannot be done. "A reference may be said to teach away when a person of ordinary skill, upon [examining] the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant." *Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.,* 73 F.3d 1085, 1090 (Fed.

[1] *See In re Ratti*, 270 F.2d 810, 813 (CCPA 1959) ("This suggested combination of references would require a substantial reconstruction and redesign of the elements shown in [the primary reference] as well as a change in the basic principles under which the [primary reference] construction was designed to operate."); MPEP § 2143.01(VI).

Cir. 1995) (alteration in original) (quoting *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994)). Nothing in *In re Gurley* indicates that a reference "teaches away" only when the reference states that something cannot be done. The Court in *Gurley* noted that a finding that a reference "teaches away" is important but does not by itself require a conclusion of non-obviousness. *See In re Gurley* at 553 ("Although a reference that teaches away is a significant factor to be considered in determining unobviousness, the nature of the teaching is highly relevant, and must be weighed in substance.").

We agree with Appellants that Katsuki, considered as a whole, teaches away from the arrangement required by claim 15. Katsuki's description of the prior art and the noted advantages of arrays of control/memory units corresponding one-to-one to the processor units (e.g., Abstract; col. 6, ll. 32-30; col. 7, l. 23 - col. 8, l. 13; col. 16, ll. 40-48; all claims (claims 1 and 14 independent)) would lead one of ordinary skill in the art away from using one state control unit for a plurality of processor elements as claimed. Katsuki thus at the least teaches away from the claimed invention.

Further, on this record, we agree with Appellants that modifying Katsuki in a way contrary to the teachings set forth in the reference fails to demonstrate prima facie obviousness of the subject matter of claim 15. The "teaching away" of Katsuki in this case is a highly relevant factor to be accorded substantial weight in the analysis of patentability. The evidence of obviousness in the present case does not outweigh, by a preponderance, the evidence of non-obviousness. We therefore cannot sustain the § 103(a) rejection of claim 15.

Appellants submit that claim 21 contains a feature similar to that of claim 15, in that claim 21 recites that "the multiplicity of said processor elements is divided among a number of element areas corresponding to the number of said plurality of state control units, said number of element areas being less than said multiplicity of processor elements."

The Examiner does not respond to Appellants' above-noted argument with respect to claim 21. Moreover, the statement of the rejection of claim 21 (Ans. 5-6) is deficient because the rejection fails at least to identify the differences between the claim and the prior art. In any event, we do not find sufficient teachings for the argued feature of claim 21 at the indicated text, whether the citations are intended to refer to Katsuki or to Stokes.

We therefore cannot sustain the § 103(a) rejection of claim 21. As claims 22 through 35 depend from claim 21 and May as additionally applied to dependent claims does not remedy the basic deficiency in the rejection, we cannot sustain the § 103(a) rejections of claims 22 through 35.

DECISION

The Examiner's § 103(a) rejection of claim 9 is affirmed. The Examiner's § 103(a) rejections of claims 15 and 21-35 are reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 41.50(f).

AFFIRMED-IN-PART

pgc